IN THE SPECIFICATION

Please amend paragraph [0045] with the following:

[0045] A second mask layer 281 is then placed over the top of the dielectric spacer material 275 and patterned to open slots in the mask layer 281 over the cell source regions 240. For another embodiment, second mask layer 281 and the mask layer of Figure 2B are patterned with the same pattern. As described in United States Patent No. 6,309,975, ions are then implanted into the exposed polysilicon 290, as shown in Figure 2E. Examples of the implanted ion species include, but are not limited to boron, arsenic, phosphorous, argon, and silicon. The implant depth in one embodiment is set to be approximately one half the thickness of the polysilicon layer 285 to a selected dose level. The ion dosage level is typically selected to be in the range of $5x10^{18}/cm^3 - 5x10^{20}/cm^3$. The second mask layer 281 is then removed and the layer of polysilicon 285 is wet etched. One such chemical that can be utilized for the wet etch process is dilute TMAH. In one embodiment, the etch is a non-anisotropic etch, etching all surfaces evenly except for those surfaces that have been ion implanted. The ion implantation generates a wet etch selectivity (a slower etch rate) between the implanted polysilicon film 290 and non-implanted polysilicon film 285. This allows the non-implanted polysilicon 285 to be etched away and leave the implanted polysilicon 290 local interconnects coupled to the source region 240, as shown in Figure 2F. In one embodiment, the second layer of photo resist is patterned and the polysilicon layer 285 is ion implanted such that a "T" shaped or a "Y" shaped local interconnect is formed in the trench that partially covers the corners of the adjacent word line stack 245. This allows the formed local interconnect to advantageously protect the spacer dielectric 275 on corners of the word line stacks 245 from potential thinning due to further processing and/or etching and has the additional beneficial effect of decreasing the resistance of the resulting local interconnect 290 by providing a larger cross sectional area. In addition, the T or Y shape also improves the edge definition of the local interconnect and limits undercutting of the local interconnect during etching. Contact formation to the local interconnect, and current carrying capacity of the interconnect line are promoted, and interconnect resistance is reduced by this interconnect shape. It is also noted that the word line cap 230 formed in one embodiment of the present invention increases insulation available on the top of the word line stack 245. This

helps improve the insulation of the word line 245 and mitigates any stair step formation in the spacer insulation due to etching during the formation of the local interconnect.